Design of an Energy Efficient Half Adder, Code convertor and Full Adder in 45nm CMOS Technology

Sameer Dwivedi, Dr. Neelam Rup Prakash

Abstract— CMOS Technology has been evolved greatly in past and the designing of the circuits depends directly on the technology one uses. Electronic system consists of a number of block elements which forms the base of the circuit and the efficiency of these components will govern the overall performance of the system. Adders and Code converters are used repeatedly in the circuits requiring counting, encoding and decoding. Thus their performance needs to be high. A Novel approach has been applied for the designing of these elementary blocks using Cadence Virtuoso tool for simulation.

Index Terms— XOR gate, Half Adder,Full adder,Code-convertor, Power and delay analysis, CMOS invertor -Pass transistor logic,minimum transistor count circuits.

1 INTRODUCTION

Low-power VLSI system designing is essential because of the rapid growth in Tele-communication, Digital signal processing (real time analysis) and others. System designing is entirely depends upon the basic building blocks with their proper arrangements in order to have lesser delays and low power consumption. In general, the three basic criteria which need to be observed while designing are Power, Area and Speed. Area and Speed depends upon each other as variation in one leads to changes in other factor.

Full adders are the basic cell in various circuits which is used for operations such as addition, multiplication, address calculation etc. Enhancing the performance of Full adder will have direct effect on the performance of the whole system. Thus, designing a 1-bit Full Adder cell with lesser delay, low power consumption and higher performance is needed [1]. XOR gates are the fundamental building block of Full adder [2]. If the performance of the XOR gate is improved then significant improvement in the performance of the adder can be achieved. In order to design a low power circuit, the minimum voltage i.e. Threshold voltage, need to be as low as possible and the most effective way to reduce the threshold voltage in deep-sub micrometer region is by varying W/L ratio of transistors and scale down the supply voltages. Full Adders can be designed using a number of different techniques including pass transistor logic, conventional gate method, 14-T designs, Complementary pass transistor based design, Transmission Function Full Adder (TFA), Transmission Gate Adder (TGA), Complementary CMOS Full Adder, Hybrid cell Full Adder, Bridge circuit design, Double pass transistor Full Adder and others in different nano metres ranges.

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2 RELATED WORKS

Adders are the elementary component of all the arithmetic units and the efficiency of adder circuits defines the performance of circuits like multipliers, processors, arithmetic logic units etc. Full Adder has been transformed from conventional 28 transistors to 10 transistors and the researchers are still working on new technologies to design low power and lesser transistor count adder circuits. With technology scaling, the CMOS technology is now in sub-micron region and thus power dissipation and average power consumption for compact circuits is of high importance. XOR and AND gates are used in the designing of half and full adders. The proper working of these two basic components defines the efficiency of adder circuits. A lot of work had been done on these basic components and still great emphasis has given to these building components. Conventional XOR gate was designed using 16 transistors and today the same can be designed using 5 transistors only. Hence, the hardware design has been changing with advancements in techniques and technology and this leads us to design low power and lesser elementary components.

3 PROPOSED WORK

In this paper, lesser transistor count half and Full adders have been designed. This requires XOR and AND gate to be design with least transistor count. Here, a 3-transistor based XOR gate and 1-transistor based AND gate is designed which leads us to a 4-transistor half adder and 8-transistor full adder circuits.

3-T based XOR-Gate design: XOR gate is one of the fundamental gate used in circuit designing. Its working is such that the output will be high only if given two inputs are of opposite logic levels i.e. when one of the inputs is high and other is low or vice versa and output will be low if two inputs are of similar logic level. It is the building element for half and full adders. A high performance and minimum power consump-

tion XOR gate can be designed by using an approach of pMOS pass transistor along with a conventional CMOS inverter [3]. This approach involves the uses of just 3 transistors for getting the desired output. The model is shown in fig.1 and the working principle is such that when the input A1 is at logic high, the first pair of pMOS and nMOS will work like CMOS inverter. Therefore the output Y is the complement of input A2. When the input A1 is at logic low, the transistor M1 and M2 output is at high impedance. However, the pass transistor M3 is enabled and the output Y gets the same logic value as input A2. Hence, the working as an XOR gate is achieved. However, a drop in threshold occurs across transistor M3 in one case and consequently the change in output will take place. The phenomenon is called voltage degradation and can be minimized by increasing the Aspect ratio (W/L) of transistor M3 [4].

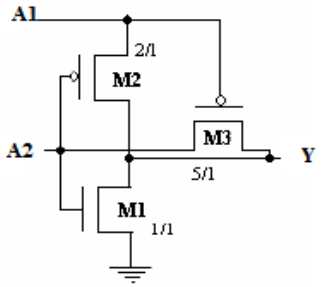

Figure 1: 3-T based XOR gate circuit.

The threshold voltage can be managed by changing the Width of pMOS and nMOS used in circuit and that too in different variations. Like the pMOS of inverter stage can have a different aspect ratio while the nMOS have different. As the final stage consists of pMOS pass transistor, a lot of variation in the output depends upon it. Thus, a larger increase in its width will be considered. Typically used Aspects ratio are 1/1 or 3/1 for nMOS of inverter, 2/1 or 3/1 for pMOS of inverter and 3/1 or 5/1 for the pMOS pass transistor.

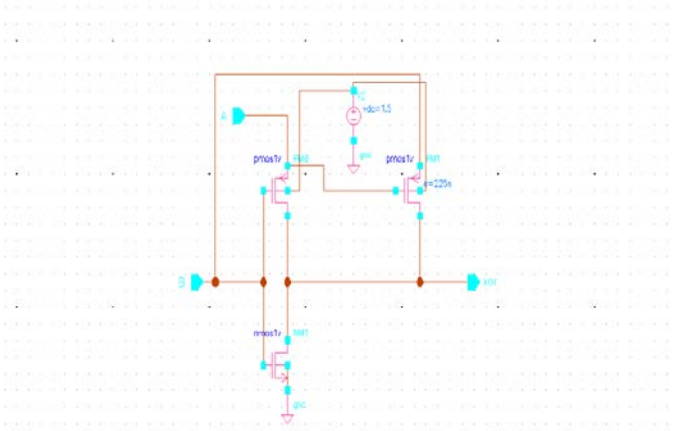

Figure 2: Schematic of 3-T XOR gate

1-T based AND GATE: AND gate is a basic digital logic gate that implicates logical conjunctions- it behaves according to the truth table given below. A high output (1) results only if both the inputs to the AND gate are high (1). If neither or only one input to the AND gate is high, a low (0) output results. In other sense, the function of AND effectively finds the minimum two binary digits, just as the OR function finds the maximum. Therefore, the output is always '0' except when all the inputs are '1' [5].

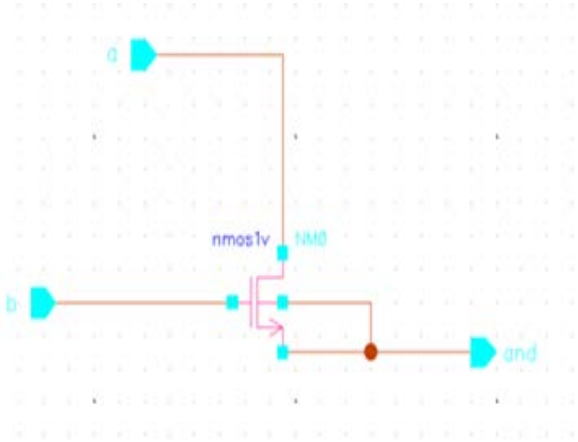

Figure 3: Schematic of 1-T AND gate

4-T based HALF ADDER: Half Adder circuit is used for adding two-bits and gives output as sum and a carry. A number of systems require the addition of less number of bits in a staged form and there half adders can be used efficiently. Half Adder is a combination of XOR gate and a AND gate. The work has been carried out by using a 3-T XOR gate and a single CMOS pass transistor based AND gate [6].

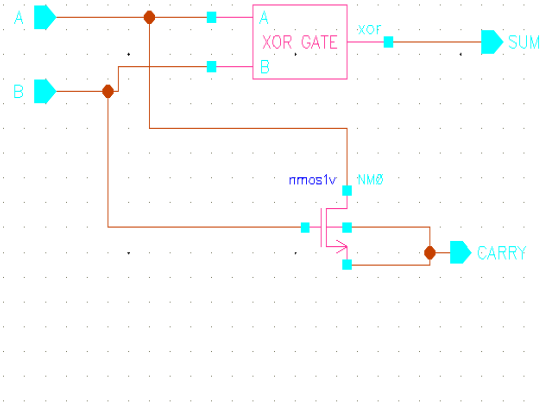

Figure 4: Schematic of 4-T Half adder circuit

CODE CONVERTOR: Code Convertors are repeatedly used in digital circuits. A number of conversion available but the most widely used one is Binary-to-Gray code (BCD) convertor. A BCD can be designed efficiently by using XOR gates and their conversion is based completely on the principle of XOR gate.

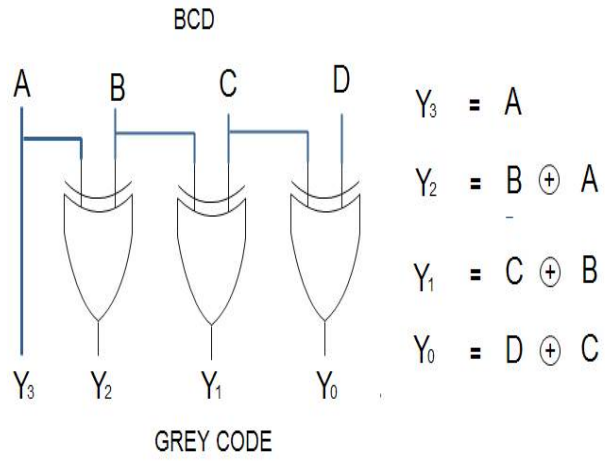

Figure 5: Symbolic representation of BCD-to-Gray code convertor

8-T based Full Adder: Full adder is used to add three bits and gives the output as Sum and Carry. Its working determines the overall performance of a number of systems. 1-bit full adder is one of the most important components of a processor that determines its throughput [7]. A Full Adder can be designed using a number of different techniques like conventional approach, using pass transistor etc. Here an 8-T based 1-bit Full adder is designed whose average power is less than the standard Full adder cell. Full-adder comprises of two staged XOR gate using CMOS inverter and pass transistor logic [8].

The Carry has been taken out using the similar pass transistor logic. Two pMOS works as pass transistor for Sum and two for Carry. The conventional Full adder is basically a two staged Half adder but if designed using given approach, the number of transistors used will be reduced that will directly affect the performance in a better way[9].

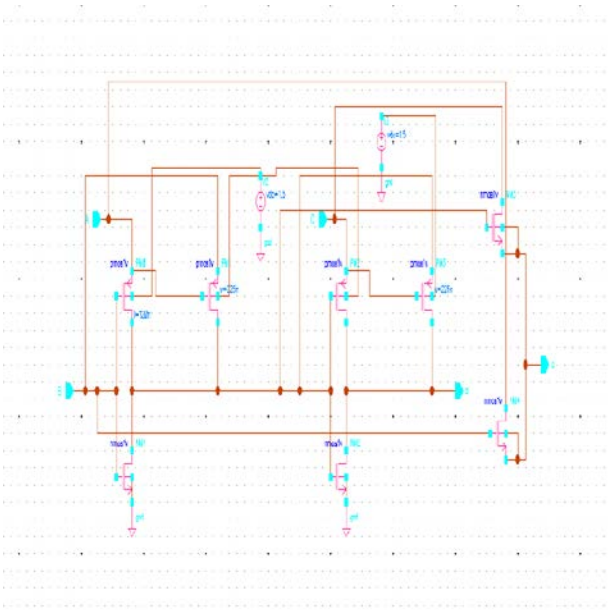

Figure 6: Schematic of 8-T Full adder circuit

4 SIMULATION RESULTS

This chapter contains the simulation screenshots of PTL logic based AND gate, 3-T based XOR gate, 4-T based half adder, 8-T based Full adder. Simulation purpose followed by design synthesize is carried out using Cadence Tool. The results are shown in the terms of time delay and average power. At the end of this chapter, a concluding table is also given.

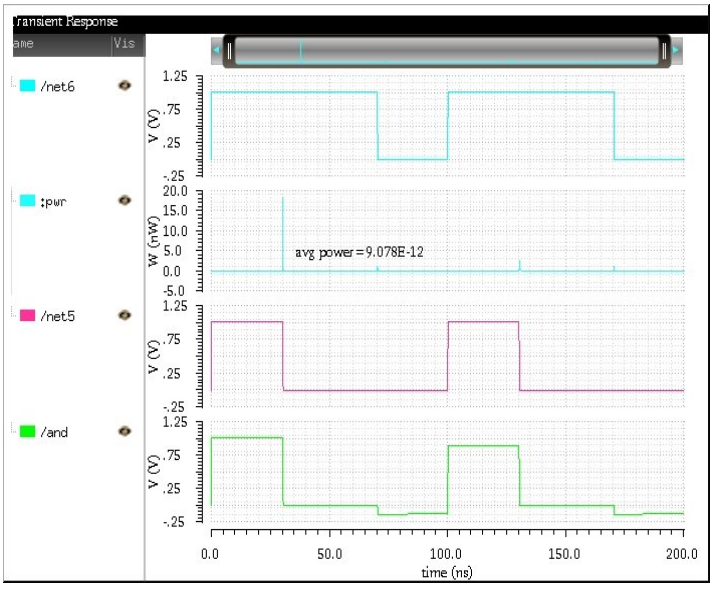

Figure 7: Simulation analysis of PTL logic based AND gate

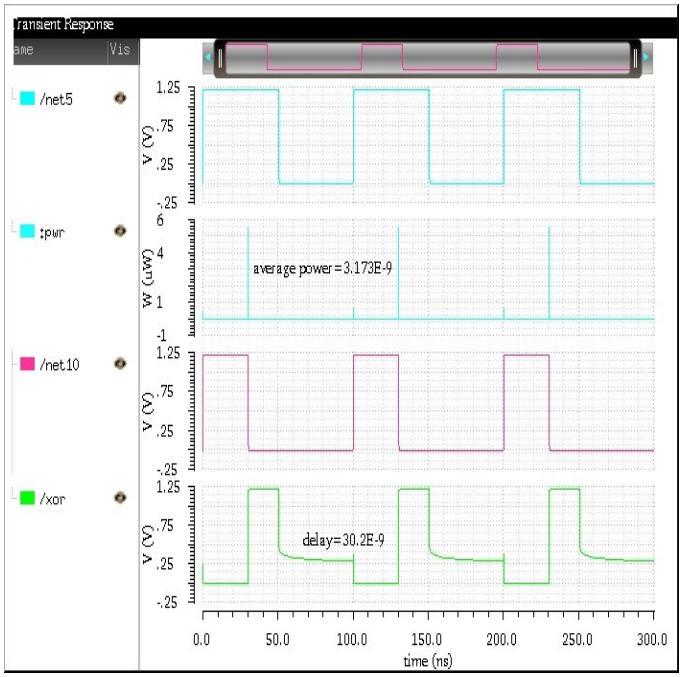

Figure 8: Simulation analysis of 3-T XOR gate

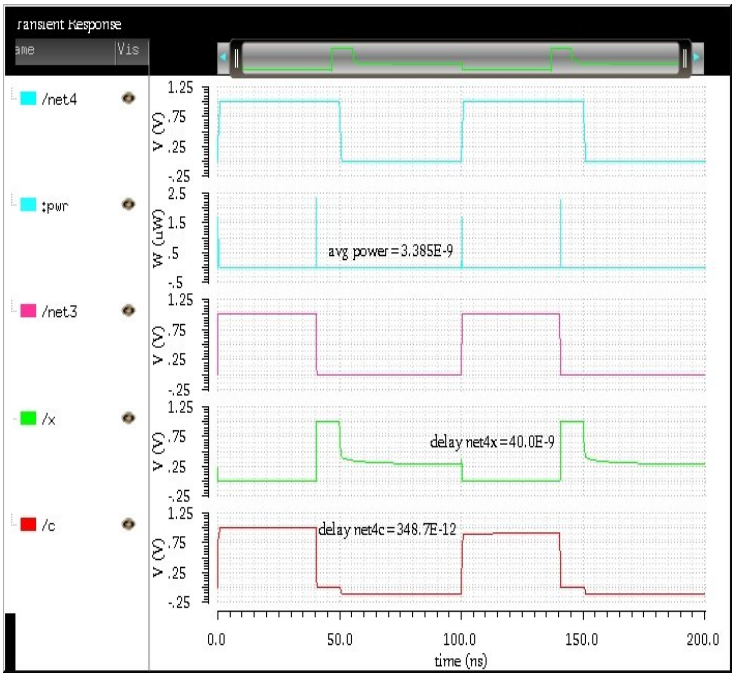

Figure 10: Simulation of 4-T Half Adder

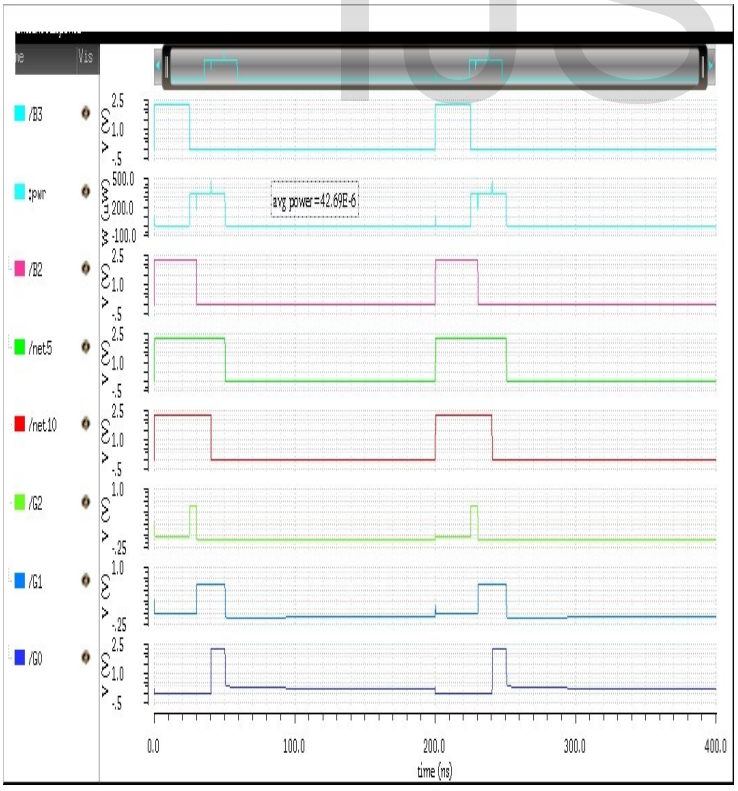

Figure 9: BCD-to-Gray convertor simulation

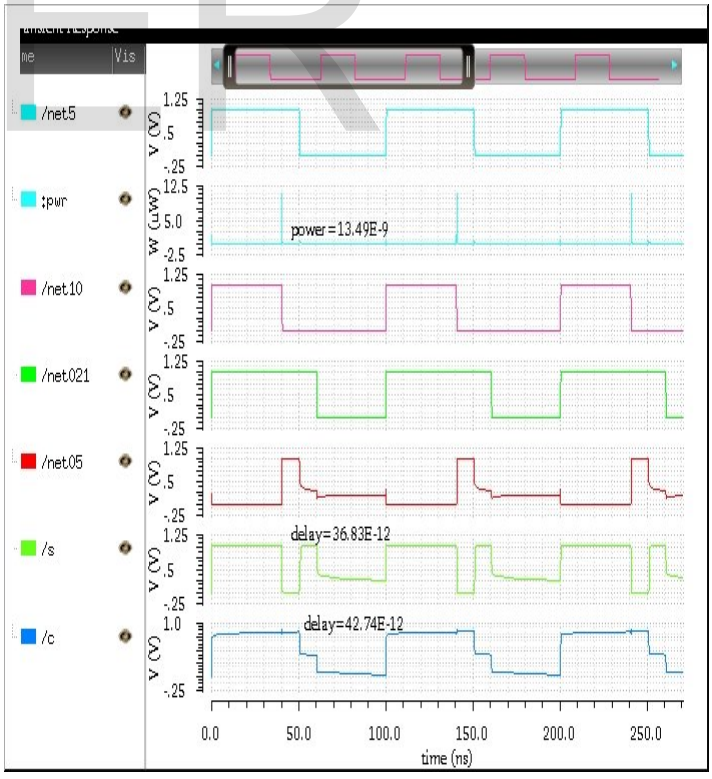

Figure 11: Full Adder simulation at supply voltage of 1.8 V and input voltages at 1.5 V.

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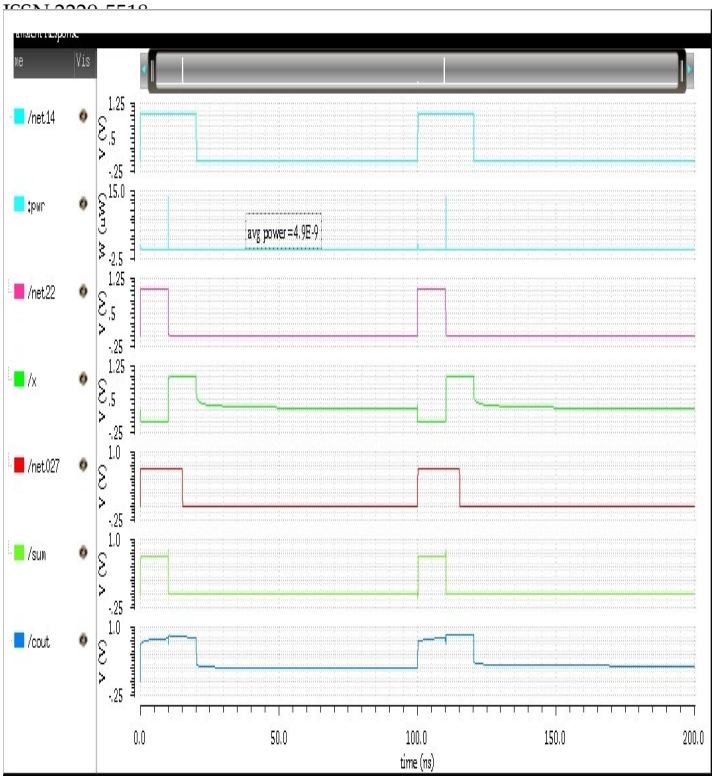

Figure 12: Full Adder simulation at supply voltage of 1.5 V and input voltages at 1.2 V.

5 CONCLUSIONS AND FUTURE WORK

Adder is the most prominent low power consumption cell. Use of efficient half adder, Code converters and Full adders will significantly decrease the power consumption in electronic circuits. As the problem of voltage degradation has been seen, a better approach is varying the W/L ratio of different transistors up to a certain limit so that the threshold voltage can be minimised and a more identical output can be achieved. Designing of a high speed and low power adder has been done by synthesizing on Cadence RTL Compiler. VLSI Design of conventional and designed adders has been achieved at schematic level. Simulations and synthesis are recorded. Comparison of the results for the adders shows that there is a considerable reduction in delay and power. This design can be used for high speed and low power consumption applications where area is not a major issue.

The power requirement can be further reduced by using low power elementary components and to achieve faster circuit operations, new and constructive algorithms have to be considered.

References

[1] A.M. Shams and M. Bayoumi, "A novel high-performance CMOS 1- Bit full-adder cell," IEEE Trans. Circuits Syst.-Part II, vol. 47, pp 478-481, May 2000.

[2] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," in *Proc. IEE Circuits Devices Syst.*, vol. 148, pp. 19-24 Feb. 2001.

[3] J. Wang, S. Fang, and W. Feng, —New efficient designs for XOR and XNOR functions on the transistor level, IEEE J. Solid-State Circuits, vol. 29, no. 7, pp. 780–786,JulY 1994.

[4] R. Zimmermann and W. Fichter, —Low –power logic styles: CMOS versus pass-transistor logic, IEEE J. Solid-State Circuits, Vol. 32, pp.1079-90,July1997.

[5] N. Weste and K. Eshraghian, —Principles of VLSI Design, A System Perspective, Reading, MA: Addison-Wesley, 1993

.

[6] Shital Baghel, Pranay Kumar Rahi, Nishant Yadav, 2015, "CMOS Half Adder Design & Simulation Using Different Foundry", Internation al Journal of Innovative Science, Engineering & Technology (IJISET), Vol. 2 Issue 3, pp 195-198.

[7] H.T. Bui, Y. Wang, Y. Jiang , "Design and analysis of 10-transistor full adders using novel XOR–XNOR gates," in *Proc. 5th Int. Conf. Signal Process.*, vol. 1, pp. 619–622, Aug. 2000.

[8] S. Goel, A. Kumar, M. A. Bayoumi, —Design of Robust, Energy-Efficient Full Adders for Deep-Sub micrometer Design Using Hybrid-CMOS Logic, IEEE Transactions on VLSI 2006.

[9] A. A. Khatibzadeh and K. Raahemifar, —A Study and Comparson of Full Adder Cells based on the Standard Static CMOS Logic, IEEE CCECE 2004 -CCGEI 2004, Niagara Falls, May 2004.

Table 1: Comparison table of designed hardware components

Circuit Implemented	Design Style	Transistor Count	Power	Delay
XOR gate	Conventional	16	18.416 uW	73.6 ns
	3-T	3	5 nW	30.2 ns
Binary to Gray Code Convertor	9-T	9	42.69 uW	93.6 ns
Half adder	Conventional	12	4.99 uW	----
	7-T	7	1.81uW	Sum = 137.8 ns
				Carry = 83.5 ns
	4-T	4	3.3 nW	Sum = 40 ns
				Carry = 348.1 ps
Full adder	Conventional	28	29.3 uW	-----
	14-T	14	7.2 uW	-----
	10-T	10	1.32 uW	-----
	8-T (input voltages =1.5 V)	8	13.49 nW	Sum = 36.8 ps
				Carry = 42.7 ps
	8-T (input voltages =1.2V)	8	4.9 nW	Sum = 39.5 ps
				Carry = 41.65 ps